

B: Amendments to The Claims:

What is claimed is:

1 1. (Currently Amended) A method of automatic delay detection
2 and receiver adjustment for a synchronous communications bus
3 system with multiple cycle delays, the method comprising the
4 steps of:

5 (a) defining a delay detection and calibration
6 phase for said synchronous communications bus system with
7 multiple delays over multiple bus lines;

8 (b) sending during said delay detection and
9 calabration phase a predefined bus signal test pattern for
10 each bus line ~~during the delay detection and calibration~~
11 ~~phase;~~

12 (c) using the predefined bus signal test pattern
13 to determine a longest delay time for each bus line of said
14 multiple bus lines during the delay detection and
15 calibration phase;

16 (d) adjusting a receiver for each bit line of
17 said multiple bus lines to receive incoming signals for each
18 bus line at a time based on the determination of step (c);
19 and after the detection and calabration phase is complete,

20 (e) placing the bus system in a normal
21 communication mode.

1 2. (Currently Amended) In a synchronous
2 communications bus system having a sender subsystem and a
3 receiver subsystem having multiple bus lnes, comprising:

4 an apparatus for detecting delay and adjusting all
5 receivers in the receiving subsystem having multiple bus
6 lines, the apparatus including comprising:— worst case
7 delay detection circuitry for each bit of the receiving
8 subsystem bus lines system; and



9 control circuitry coupled to the worst case delay
10 detection circuitry for each bit; operative to select one of
11 two receiver paths for each bit as a function of each bit's
12 delay detection circuitry output and clock signals
13 associated with each bit's receiver latch in the receiving
subsystem.

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2 3. (Original) The apparatus of Claim 2 wherein at
3 least two of the bits have worst case delay detection
4 circuitry adapted to use different clock phases of the
synchronous bus system.

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